SPECIFICATION

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RF Energy Dispersal in Systems Consisting of Aggregated Computing Elements As Subsystems

Background of Invention

[0001] This invention pertains to the aggregation of computer systems and other devices requiring a clock or oscillator and, more particularly, to the mitigation of electromagnetic interference of the aggregation.

[0002] Devices that have embedded oscillators or clocks inherently emit electromagnetic energy. The energy is emitted at frequencies related to the fundamental frequency of the oscillator or clock. This emitted energy is both undesirable and parasitic to other devices. The related frequencies can be of any component of the oscillator frequency including the fundamental frequency and any harmonics thereof. The harmonic components of the fundamental frequency occur at multiples of the fundamental and at sums and differences between any two or more components.

[0003] Devices which have embedded oscillators or clocks require testing for compliance to several government agencies" established requirements. One such agency is the Federal Communications Commission. The established requirements maintain that emissions for any given device remain below a given threshold. The threshold corresponds to an amount of energy per predefined frequency bandwidth which energy could reasonably interfere with a neighboring device. The testing device used in order to determine compliance is usually a spectrum analyzer which sweeps all frequencies of interest and which reports the detected level of emissions per the predefined bandwidth throughout the sweep of frequencies.

[0004] Devices are currently produced with a fixed set of one or more oscillators which function as time keepers or clocks. These devices usually take the form of an electronics board assembled in a case with other ancillary parts and creating a working device. As singular elements, each completed device is certified to comply with the defined set of government agency requirements. When clustering and operating more than one of these devices in close proximity, the result is an integrated higher level system. It is this integrated system, the aggregation, when operating, that cannot be expected to meet the original agencies" criteria for each of the elements it is composed of. The problem is that the aggregation of systems generally exceeds the allowed energy / frequency levels set by one or more agencies.

Summary of Invention

[0005] An aggregation of devices is provided in which a subset or all of the devices are designed to operate in close proximity of each other. The subset or all of the devices are provided with a programmable oscillator or clock. The devices are linked through an inter-device link. Each proximate device contains a clock frequency controller which couples the inter-device link and the programmable oscillator or clock and which controls the frequency of the programmable oscillator or clock. The frequency of each proximate device is set to operate at a unique operating frequency. Each unique frequency is set to differ from each other by at least a predetermined frequency differential.

Brief Description of Drawings

[0006] Some of the purposes of the invention having been stated, others will appear as the description proceeds, when taken in connection with the accompanying drawings, in which:

[0007] Figure 1 is a block diagram of a computer system for use in conjunction with the current invention.

[0008] Figure 2 is a block diagram of a computer system for use in conjunction with the current invention having a set of spread spectrum clocks.

[0009] Figure 3 is a block diagram of a system consisting of aggregated computing elements as subsystems.

[0010] Figure 4 is a block diagram of a system consisting of aggregated computing elements as subsystems with one of the computing elements functioning as a master device and the remainder of computing elements functioning as slave devices.

[0011] Figure 5 is a process flow diagram showing the selection and modification of the operating frequency of a device operating in the master mode.

[0012] Figure 6 is a process flow diagram highlighting the frequency modification mode of a slave mode device.

Detailed Description

[0013] While the present invention will be described more fully hereinafter with reference to the accompanying drawings, in which a preferred embodiment of the present invention is shown, it is to be understood at the outset of the description which follows that persons of skill in the appropriate arts may modify the invention here described while still achieving the favorable results of this invention. Accordingly, the description which follows is to be understood as being a broad, teaching disclosure directed to persons of skill in the appropriate arts, and not as limiting upon the present invention.

[0014] Although several of the illustrative embodiments are aggregations of computer systems, it should be kept in mind that the invention is not limited to computer systems and is applicable to other aggregations including switches, routers, hubs, and in general to the aggregation of any system or device which operates based on a clock or oscillator and which emits electromagnetic interference as a function of this clock or oscillator.

[0015] Referring now more particularly to the accompanying drawings, Figure 1 illustrates one type of computer system 100 utilized for the implementation of one embodiment of this invention. In this embodiment, an aggregation of proximate computer systems utilizing the design of computer system 100 is formed. Each computer system 100 implements a bus programmable clock 101 via a bus programmable clock generator 102. The bus programmable generator 102 receives programmable frequency commands through computer system bus 104. The frequency is controlled by clock controller 105 within the system acting by some

predetermined set of steps implemented in hardware, software, or a combination of hardware and software. The steps can also include manual steps to be controlled by a user / operator. Optionally, under the control of the clock controller 105, a display (not shown) can be used to display a user prompt and solicit input from the operator and accept user input through a user input device such as optional keyboard 106. Bus controller 108 controls all bus functions and further couples optional keyboard 106. Computer system 100 communicates to other computers through communicating agent 109 from which frequency commands can be transmitted and received. Bus programmable clock 101 can be used directly as the system clock and can also be used as a basis for a series of derived clocks for implementing other functions 110. Other functions 110 can include video, memory, I/O bus, and other intermediate clocks.

[0016] Figure 2 depicts a computer system 200 which functions similarly to the computer system 100 of Figure 1. Computer system 200 further implements a spread spectrum clock 202. A spread spectrum clock is a clock whose frequency varies relatively slowly and continuously. In general a spread spectrum clock requires a stable base frequency as in bus programmable clock 101. Spread spectrum controller 201 uses bus programmable clock 101 as a reference signal and operates on it so as to provide outputs which vary in frequency by a certain percentage. Spread spectrum controller 201 can be implemented using any industry standard spread spectrum modules.

[0017] Figure 3 shows an aggregation 300 of like computers 100a, 100b, and 100c which are designed and tested to operate in close proximity of each other. Computers 100a, 100b and 100c may be installed, either proximate to each other in separate housings, or installed into a common housing. Normally each computer 100 is tested to not exceed certain government agency limits on radiated and/or conducted electromagnetic energy. Each of like computers 100a, 100b, and 100c initially operates at the same factory default clock frequency setting. As a result, aggregation 300 emits undesirable electromagnetic emissions which sum at the fundamental frequency and at the harmonic frequencies of the default factory setting. Aggregation 300, therefore, cannot be expected to also pass the same government agency tests. This is so, although to a lesser extent, when computers 100a, 100b, and 100c utilize the spread spectrum design of computer system 200.

[0018] To preclude the summation of undesirable electromagnetic emissions, each of the computer systems 100a, 100b, and 100c are set to operate at different frequencies such that no summation of fundamental frequencies and their harmonics occurs. These frequencies are all within a nominal frequency range as required by the circuits but differing by a selected frequency increment resulting in a dispersal of available energy at the nominal fundamental frequency as well as the higher harmonics of the fundamental frequency. The absolute fundamental frequencies of clocks / oscillators of computer systems 100a, 100b, and 100c are separated from each other by an amount as high as the detecting bandwidth of the measuring device. In general these measuring devices are implemented as spectrum analyzers. The theory of these analyzers is that the measured energy is the integrated average sum of the RF energy at all possible discrete frequencies within the analyzer's predefined bandwidth. Any RF energy that is higher or lower than the predefined bandwidth is greatly diminished and effectively not detected. By using RF energy dispersal in systems consisting of aggregated computing elements as subsystems, the need for special or additional RF shielding is precluded. Current design and manufacturing techniques can continue to be used, thus reducing the overall cost to implement aggregated systems.

[0019] For example, if aggregation 300 is comprised of twenty four computer systems each operating nominally at 75 MHZ, the system clock generators 102 could have a dispersal range of 4 MHz, incrementing in frequency by 166 kHz. Thus the absolute frequencies could start at 71.000 MHZ, followed by 71.166 MHZ, 71.333 MHZ, 73.500 MHZ and so on ending with 74.833 MHZ and 75.000 MHZ.

[0020] In aggregation 300, inter-computer links 302 provide inter-computer communication among the proximate computer systems 100a, 100b, and 100c. Inter-computer links 102 can be any form of network adapter or other I/O subsystem such as an Ethernet adapter card, a Token Ring adapter card, an RS-485 ring, or a USB connection, etc. . To allow an operator an effective means to supervising the aggregation 300, each of computer systems 100a, 100b, and 100c is provided with a system manager 301. The system manager 301 and the inter-computer link 302 together form communicating agent 109 of computer 100. Communicating agent 109 can be implemented through IBM's Netfinity Advanced System Management using a Remote Supervisor Adapter ™ in each of computer systems 100a, 100b, and 100c. In

one embodiment, when a second computer 100b is linked to a first computer 100a, using a Remote Supervisor Adapter ™ as the communicating agent 109, a command from system manager 301a is sent to the clock controller 105a to this effect. Clock controller 105a recognizes this command and issues a command to the new computer system 100b to change its factory set frequency to a predetermined different one. In another embodiment, an algorithm invoked in computer system 100a allows for the manual selection of frequencies and their harmonics which cannot be used due to external constrains.

[0021] Computer systems 100a, 100b, and 100c can also be managed by a computer system which is remote to aggregation 300 via network connection. This remote computer can act as a master or supervising computer to set the frequency of operation of computer systems 100a, 100b, and 100c. However, in the preferred embodiment, the supervising computer is one of computer systems 100a, 100b, and 100c. This is advantageous because all computer systems at one installation can be of the same design irrespective of whether they are proximate or not. In being of the same design, the computer systems can be lower in cost and take full advantage of the present invention.

[0022] In other embodiments, any of computer system 100a, 100b, or 100c can be made the master or supervising computer at any time. The designation of master can be accomplished via a network command to that effect, or via a mechanical switch on the front face of computer 100, or by software executing on any one system.

[0023] When computer systems 100a, 100b, and 100c are of like designs, clock controller 105 can act as either the master or the slave device. To act as master, clock controller 105 detects a master operating mode command from the system manager 301 through the inter-computer link 302 or through any other means such as by software executing on the computer system 100. Once detected, the master device can initiate a frequency selection mode and frequency modification mode for itself and for any and all other systems coupled through inter-computer link 302. All other systems coupled through inter-computer link 302 are treated as slave devices. When initially acting as master, the master device can maintain its current operating frequency, or can switch to a default or other frequency and then proceed to selecting

and modifying the frequencies of any or all of the slave devices.

[0024] Figure 4 shows an aggregation of computer systems 400 in which one computer system 100a has assumed the supervising master mode of operation, and the remaining computer systems 100b through 100n operate in the slave or supervised mode. Depicted are the victims 401 such as cell phones, mice and audio devices and the undesirably emitted fundamental frequencies, f00, f10, f20, ...fN0 and their harmonics, f01, f11, f21 , ...fN1, f02, f12, f22, ...fN2 and so on. When operating as master, computer system 100a selects and optionally modifies its frequency of operation according to the flowchart of Figure 5. Master computer system 100a then selects and optionally modifies the frequency of operation of each of the slave devices 100b through 100n by transmitting to each of the slave devices a frequency modify command. When operating as slave, computer systems 100b through 100n receive and optionally modify their frequency of operation according to the flowchart of Figure 6.

[0025] Figure 5 shows selection and optional modification of the operating frequency of a device operating in the master mode as implemented by clock controller 105. In step 501, it is first detected whether or not frequency selection is required for the master device. The master device can receive command over the network to reset of its own frequency. Once this command is recognized a flag is set to enter the frequency selection mode. The master device can likewise initiate this process on its own. If for any reason selection is not required then the processing flow continues at step 506. If frequency selection is required then process continues at step 502. In step 502, a decision is made as to whether or the selection will be automatic or manual. If frequency selection is not to be made automatically then process flow continues at step 505. At step 505 a user or operator manually enters frequency criteria. The criteria can be to frequencies which are acceptable or to frequencies which are unacceptable. A program can be executed to accept such user input on any computer in the network which has a keyboard 106 and a display (not shown), including the master system 100a. For example, if one of victims 401 is sensitive to the second harmonic f02 of computer 100a, a user can specify f02 as an unavailable frequency. The program can then calculate that the source of interference at frequency f02 is the oscillator of computer of 100a operating at f00. The program can therefore list

frequencies f00 and f02 as unavailable. The program running at supervising computer 100a would then select a fundamental frequency different from f00 and then proceed to step 506. If at any later time it is found that frequency f02 is again available, f02 and f00 can be added to list of available frequencies by the operator. The manual selection of frequencies based on user criteria can be implemented in a similar way by the program for each and all slave devices. If the decision of step 502 yields that selection should be autonomic, processing continues at step 503 wherein a default selection is made. At step 504, it is determined whether the selection made in step 503 is an acceptable one. Should the selection be unacceptable, processing continues at step 502. If the selection is found to be acceptable processing then continues at step 506. At step 506, a frequency of operation for the master device has been selected. A flag which signals the selection mode is reset and a flag which signals the frequency modify mode is set. In the frequency modify mode of operation the determination 506 of frequency is made relative to the actual operating frequency of master device 100a. If, as a result of executing either steps 501, 505 or 504, the frequency selected differs from the current operating frequency, processing continues at step 507. In step 507 the clock controller 105 of computer system 100a changes its operating frequency to the selected frequency by executing a bus 104 command to the bus programmable system clock 102. If however, at step 506 the selected frequency is found to be equal to the current operating frequency, then no operation occurs.

[0026] The processing of step 505 further maintains a list of all acceptable and unacceptable frequencies. Further, the frequencies maintained in the list are selected to differ in frequency according to the bandwidth of the testing spectrum analyzer. For example the frequencies can be made to differ by at least half the bandwidth of the spectrum analyzer. If the spread spectrum design of computer system 200 is utilized, the frequencies can additionally been made to differ according to the bandwidth of the spread spectrum. For example, the frequencies can be made to differ by at least half of the bandwidth of the spread spectrum.

[0027] Figure 6 highlights the frequency modification mode of a slave or supervised computer or device. The operation is similar to the frequency modify mode of the master or supervising computer or device as explained supra. A master device selects

unique frequencies of operation for any and all of the slave devices coupled to inter-device link 302. The master device can receive command over the network to initiate the setting of slave device frequencies. The master device can likewise initiate the process on its own. The master device issues a frequency modify command through the inter-computer link targeting a particular slave device. When a slave device recognizes this frequency modify command processing continues at step 606. In step 606 if the frequency specified in the frequency modify command is different from the current operating frequency, processing continues at step 607. In step 607 the clock controller 105 of a slave device changes its operating frequency to the selected frequency by executing a bus 104 command to the bus programmable system clock 102. If however, at step 606 the selected frequency is found to be equal to the current slave operating frequency, then no operation occurs after step 606.

[0028] In the drawings and specifications there has been set forth a preferred embodiment of the invention and, although specific terms are used, the description thus given uses terminology in a generic and descriptive sense only and not for purposes of limitation.